REMARKS

In the Office Action dated July 2, 2003, claims 1-24 were pending. Claims 1-24 were rejected. No new matter has been added. Reconsideration of this application as amended is respectfully requested.

In this response, no claim has been cancelled. Claims 1, 4-10, and 13-19 have been amended. Applicant reserves all rights with respect to the applicability of the doctrine of equivalents.

The Title and the Abstract of the present application have been objected to. Accordingly, a new title and a new abstract have been proposed. Applicants respectfully request the Examiner enter the proposed title and the abstract.

In addition, the Examiner objected numerous places of the specification. In this response, pages 2, 11, 14-15, 20, 29, 33-34, 36-37, 40-41, and 44 of the specification have been amended. Applicants submit that the rest of the objections to the specification are merely applicants' choice of words that have no substantial impact on the patentability and clarity of the present application.

Portions of the drawings were objected to. In this response, Figures 2, 4-7, and 9B have been amended. In Figure 2, term "(4) START PROGRAMMING" has been changed to "START PROGRAMMING". In Figure 4, texts have been added to the boxes requested by the Examiner. In Figure 5, boxes 32 has been amended to include "Spec. Prog. Mode Ccty." In Figure 6, boxes 32, 40, 62, 83, and 91 have been amended. In Figure 7, box 164 has been amended. In Figure 9B, block 317 has been amended. A copy of the above proposed figures is provided in the Appendix of this response. With respect to the terms of "circuit to send", "circuit to exit", "circuit to verify", "circuit to determine", and "circuit to reprogram", these

circuits are part of processing circuitry 33 shown in Figure 4. Specifically, on page 10 of the specification, it states:

> "Host processor 22 includes processing circuitry 33 for using a special programming mode to program memory 24. The special programming mode allows host processor 22 to send data words for programming by memory 24 and allows memory 24 to enter a special programming mode, wherein data verification is done externally by host processor 22. Circuitry 33 of host processor 22 includes circuits for performing external data verification during the special programming mode."

(Specification page 10, second paragraph).

Applicants submit that claims should be interpreted in view of the specification and drawings, and one with ordinary skill in the art would understand, based on the specification and drawings, the present invention as claimed.

Rejections Under 35 U.S.C. §112

Claims 1-24 are rejected under 35 U.S.C. §112, second paragraph as being indefinite. Accordingly, claims 1, 4-10, and 13-19 have been amended to overcome the rejections.

Rejections Under Obviousness-Type Double Patenting

Claims 1-24 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-25 of copending application No. 09/748,825 and claims 1-20 of copending application No. 09/749,133. Since this is a provisional rejection, applicants respectfully submit that a terminal disclaimer will be submitted upon the allowance or patenting with one or more claims.

Rejections Under 35 U.S.C. §103(a)

Claims 1-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over the Intel Corporation Application Note AP-629 ("AP-629") or the Intel Corporation Application Note AP-678 ("AP-678"), each taken separately, in view of U.S. Patent No. 5,600,600 of Olivo et al. ("Olivo").

Applicants submit that claims 1-24 of the present application include limitations not disclosed or taught by the cited references. Specifically, independent claim 1 recites:

> 1. A method comprising:
> enabling a special programming mode of a memory by entering a special programming access code in a state controller, wherein the memory includes automation circuitry for program verification and wherein enabling special programming mode disables internal program verification by the memory;
> programming a plurality of words into the memory during the special programming mode without the memory performing internal program verification; and
> exiting the special programming mode of the memory.

(Emphasis added).

Independent claim 1 includes limitations of enabling a special programming mode of a memory by entering a special programming mode by entering a special programming access code in a state controller, where the enabling special programming mode disables an internal program verification by the memory. Applicants submit that none of the cited references, individually or in combination, discloses or suggests the above limitations. Although AP-629 and AP-678 disclose a write state machine (WSM), they fail to disclose or suggest enabling a special programming mode of a memory by entering a special programming by entering a special programming access code in a state controller.

In addition, independent claim 1 includes a limitation where the enabling special programming mode disables internal program verification by the memory and a limitation of programming a plurality of words into the memory during the special programming mode without the memory performing internal program verification. Applicants submit that these limitations are also absent from the cited references, individually or in combination.

In the Office Action, the Examiner stated:

> "Applicant Note AP-629 also teaches that, in order to reduce programming and testing time of a nonvolatile memory, one should consider modifying the method or program flow to perform only necessary operations (see AP-629, at page 9, as well as page 10 and Figure 4). Application Note AP-629 further teaches that program verify operations initiated by external automatic test equipment (ATE) are redundant with internal program verify operations and that one can save time by not performing program verify operations (see AP-629, at page 9, column 2, e.g.).
>
> Applicant Note AP-678 similarly teaches that verification of each location as it is programmed or written should be eliminated from the programming routines of automated flash memories (see AP-678, at page 9, column 1, e.g., as well as page 10 and Figure 3), since program verify operations initiated by external automated test equipment (ATE) are redundant with internal program verify operations (see AP-678, at page 9, column 2, e.g.)."

(7/2/2003 Office Action page 14, emphasis added).

As acknowledged by the Examiner, the external verification operations by the ATE are redundant and may be eliminated. However, these sections of AP-629 and AP-678 do not read on the limitations of claim 1 set forth above, where the enabling special programming mode disables internal program verification by the memory and programming a plurality of words into the memory during the special programming mode without the memory performing internal program verification. Both AP-629 and AP-678 disclose or suggest eliminating the external verification operations. That disclosure teaches away from the amended claim 1. Specifically, the AP-629 discloses the following:

> "The flash memory internal Write State Machine (WSM) automatically verifies data written to the memory. Program verify operations initiated by the ATE are

redundant with flash memory internal program verify operations. You can save time by not performing program verify operations with the ATE."

(AP-629 page 9, col. 2, emphasis added).

That is, the AP-629 clearly discloses or suggests eliminating the external verification operations, rather than the internal verification operations as claimed by claim.

The Examiner states that:

"Olivo similarly discloses a method of programming a memory such as a flash nonvolatile memory during a "special" or test programming mode of the memory, and teaches disabling program verification operations by an internal state machine during the "special" programming mode so that a plurality of words may be programmed or tested without the memory performing internal program verification (see column 1, lines 26-62; column 2, lines 9-31; and column 4, lines 7-12 and 32-36, e.g.)."

(7/2/2003 Office Action, page 15, emphasis added).

Applicants respectfully disagree. The section of Olivo relied on by the Examiner does not disclose or suggest disabling internal verification operations during the "special" programming mode. Specifically, Olivo states:

"Consequently, having excluding the internal state machine 11, the addresses can be used freely and, using the above listed control signals with their new meaning, the desired cells can be programmed and their correctness can be verified."

(Olivo col. 4, lines 32-36, emphasis added).

Olivo further states:

"Verification is performed by a comparison of the values present after memory programming with the correct ones supplied through the data bus 3. The signal CEN also returns to a low logic value Vil and the circuit is ready to perform a new test or return to normal operation.

The test method in accordance with the present invention has the following advantages: The memory matrix test can be performed in a manner fully independent of control unit operation. The duration of the programming pulse and that of the verification phase are not bound to the internal time base and can thus be selected at will. The sequence of performance of the actual test is compatible with that used for testing EPROM memories of the known art and thus permits use of the same circuitry equipment for its performance."

(Olivo col. 4, line 63 to col. 5, line 10, emphasis added).

Applicants submit that Olivo clearly fails to disclose the limitations as amended claim 1.

The AP-629 or AP-678 does not teach or suggest a combination with Olivo, and Olivo does not teach or suggest a combination with the AP-629 or AP-678. It would be impermissible hindsight, based on Applicant's own disclosure, to combine AP-629 or AP-678 and Olivo.

Even if Olivo and AP-620 or AP-678 were combined, such a combination would still lack the limitations claimed by claim 1, which are set forth above. Therefore, for the reasons set forth above, independent claim 1 is patentable over the cited references.

Similarly, independent claim 13 includes limitations similar to those claimed by claim 1. Thus, for reasons similar to those discussed above, independent claim 13 is patentable over the cited references.

The rest of the claims depend from one of the above independent claims, thus include all of the distinct features of the respective independent claim, and therefore, for the reasons similar to those discussed above, are patentable over the cited references.

CONCLUSION

In view of the foregoing, Applicant respectfully submits that applicable rejections and objections have been overcome.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this response.

Respectfully submitted,

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